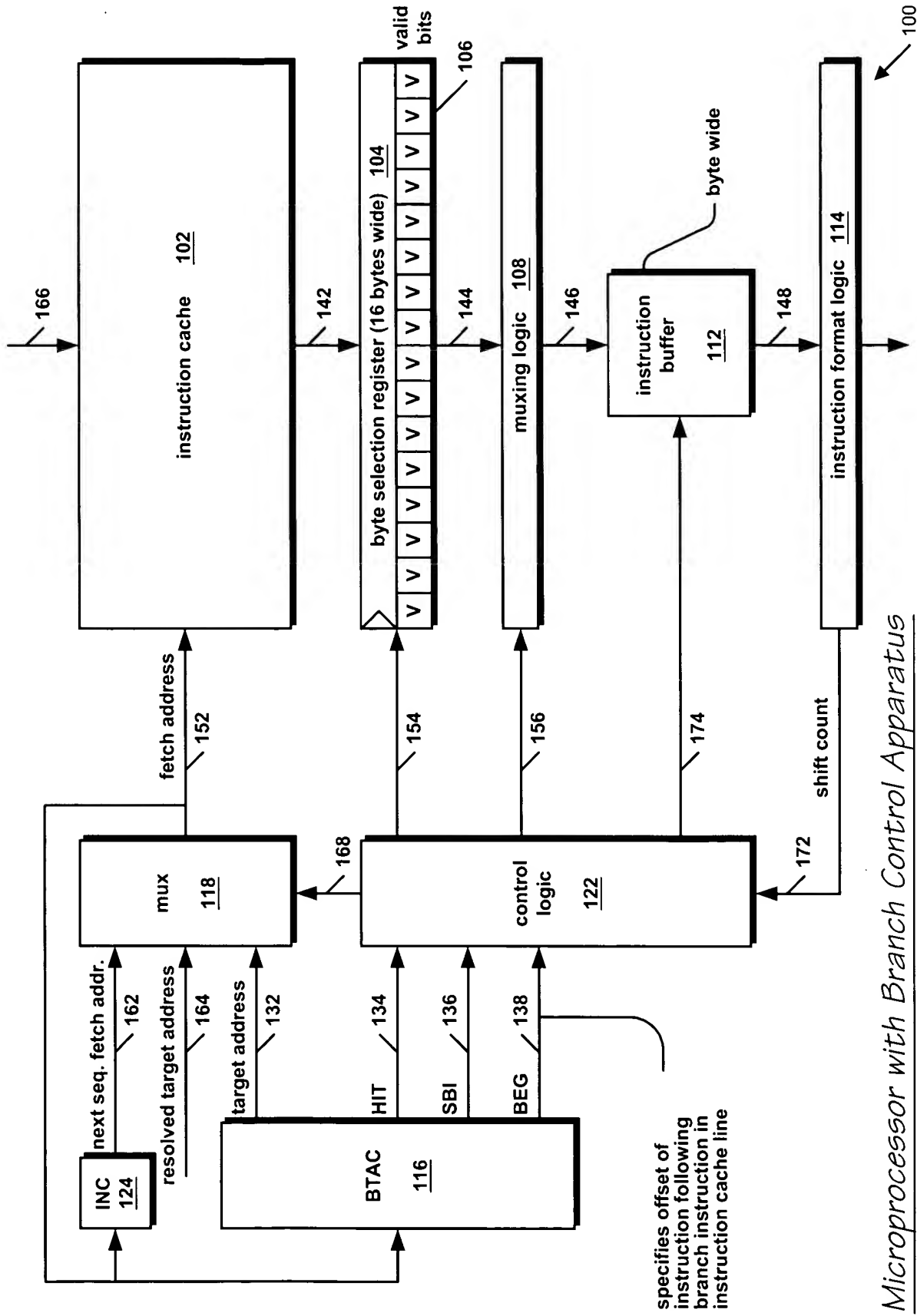
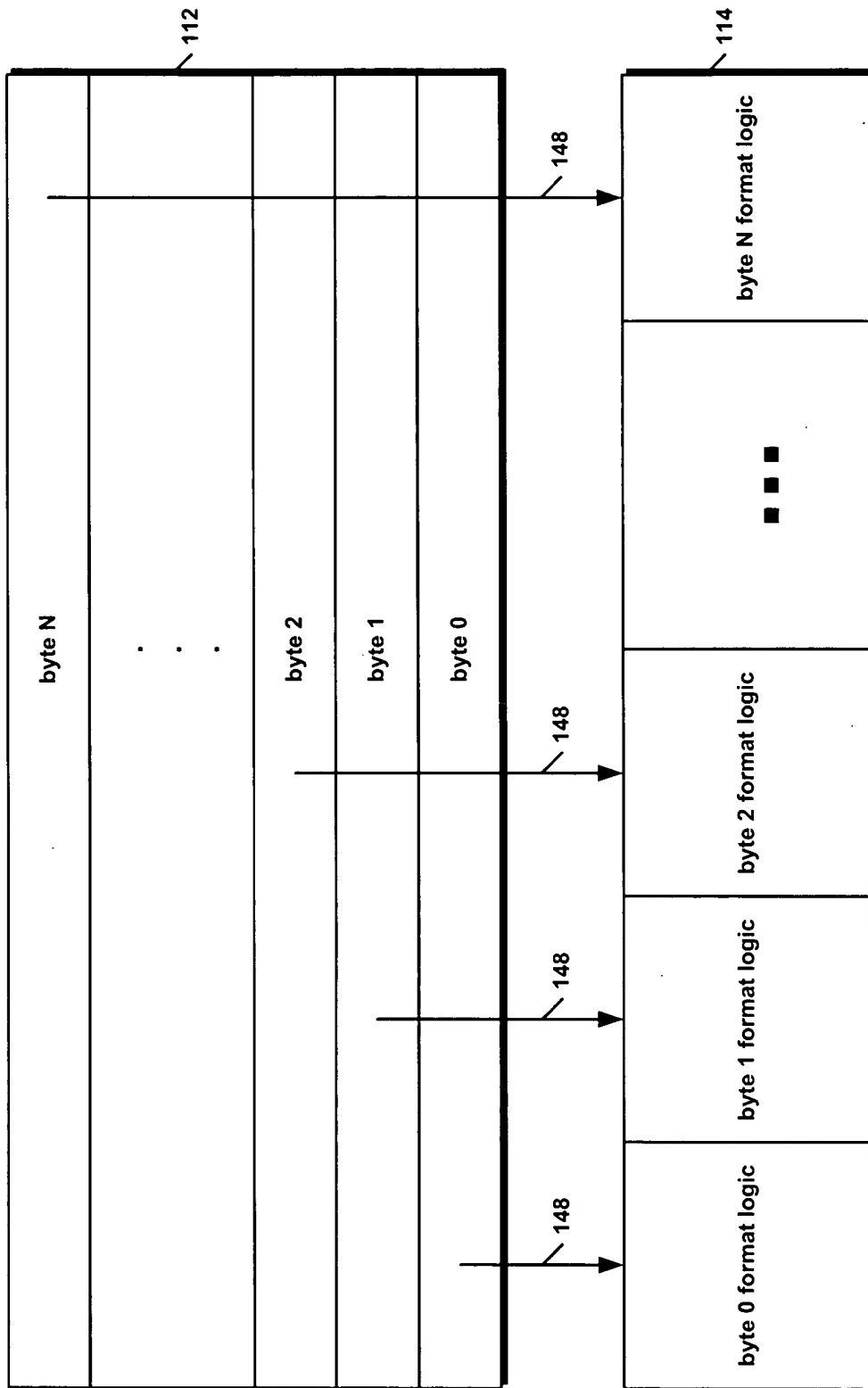


FIG. 1



Microprocessor with Branch Control Apparatus

FIG. 2



*Instruction Buffer to Instruction Format Logic Coupling*

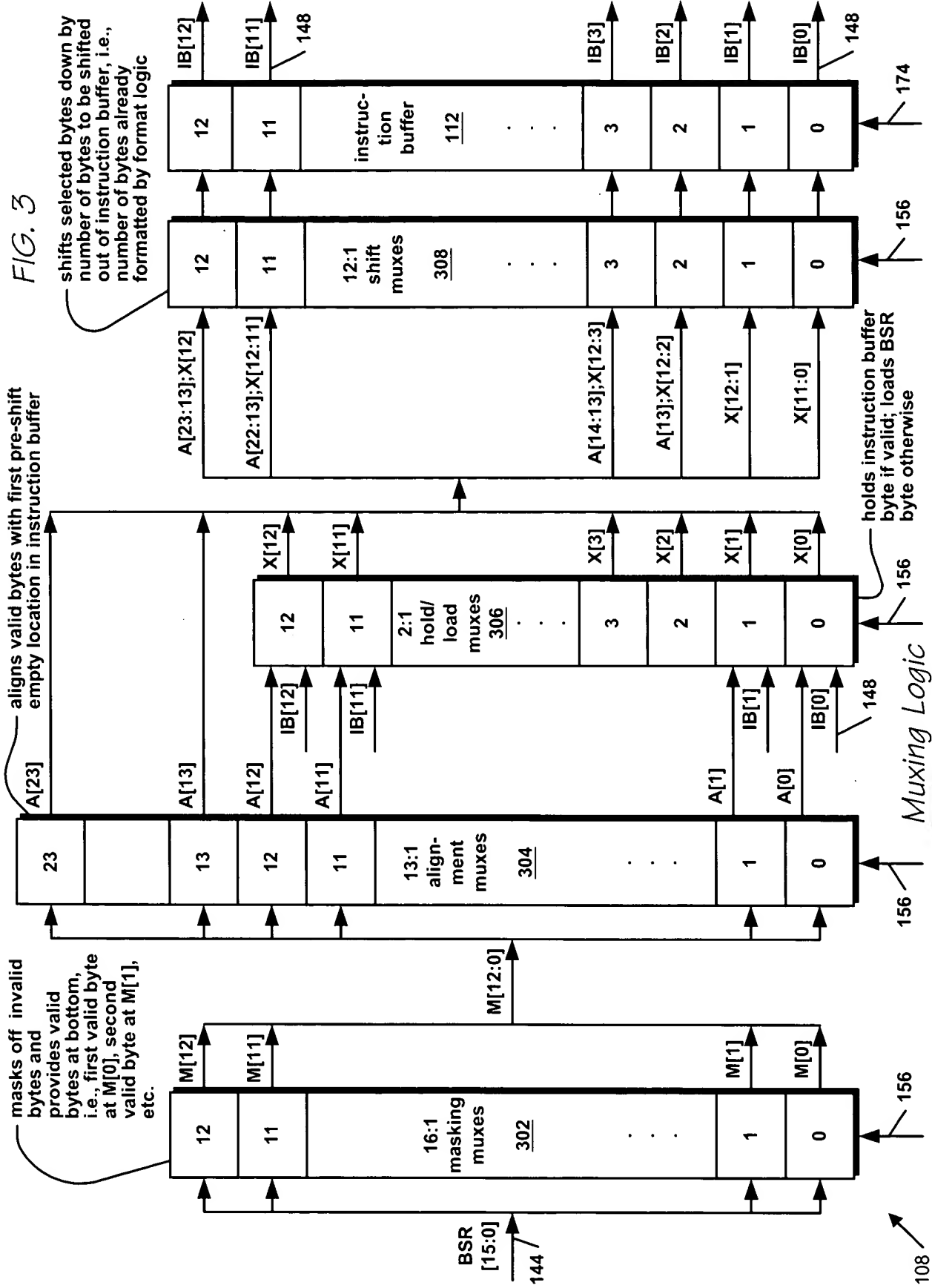
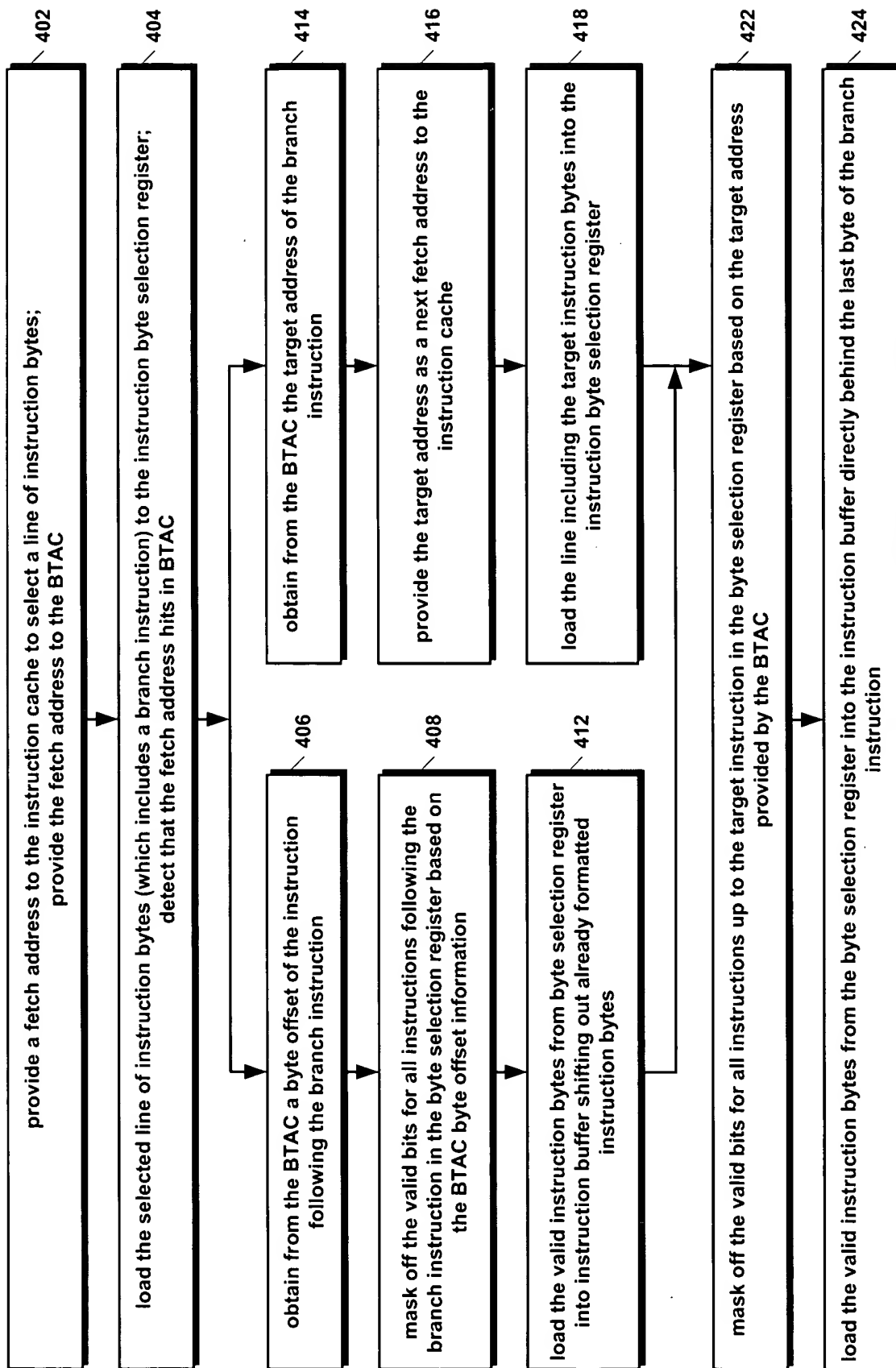
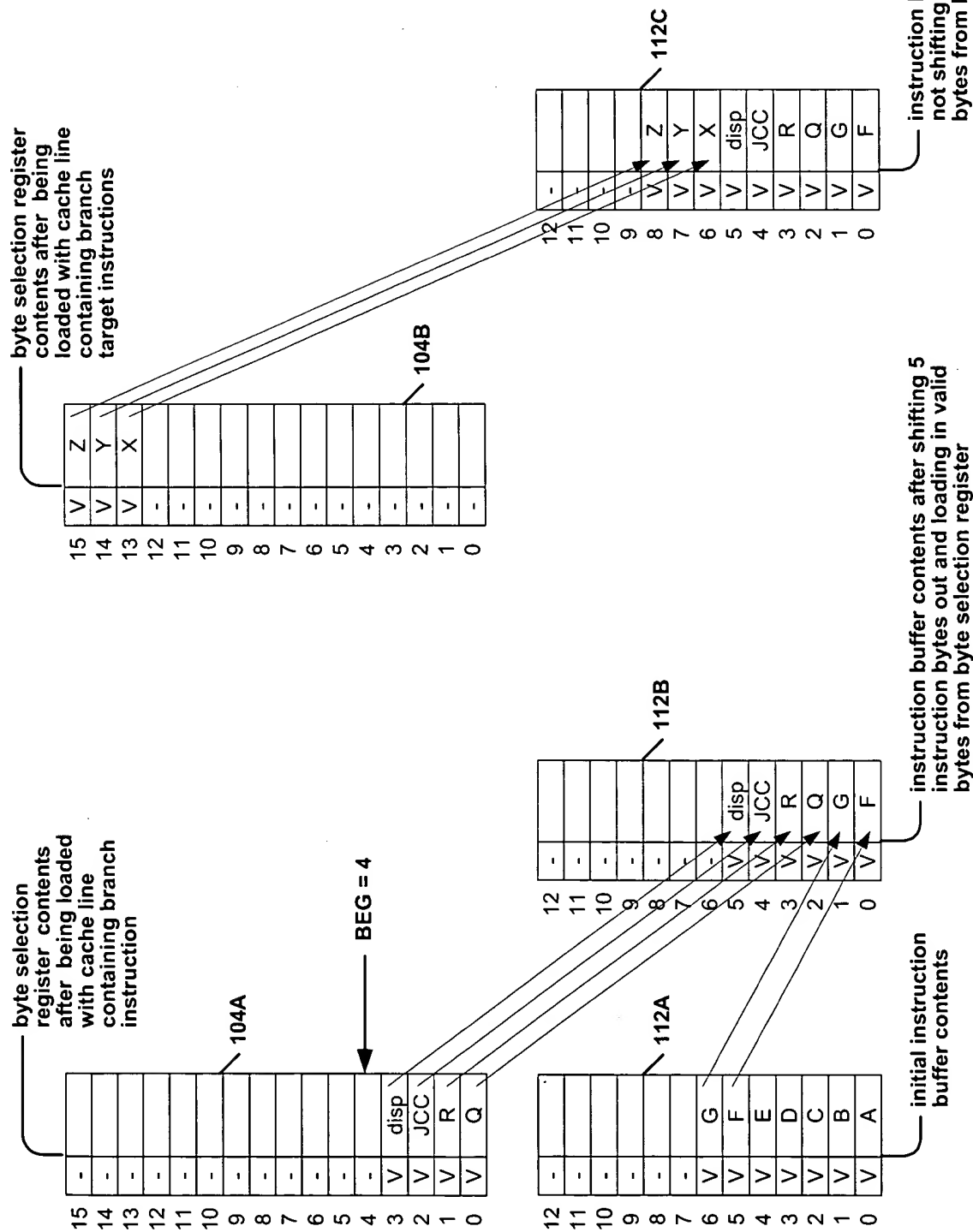


FIG. 4



*Instruction Byte Selection Method*

FIG. 5



Branch Control Apparatus Operation Example